REMARKS

This Application has been carefully reviewed in light of the Official Action issued November 3, 2008. In order to advance prosecution of this Application, Claims 1, 4, 11, 15, and 16 have been amended. Applicant respectfully requests reconsideration and favorable action in this case.

Claims 1-10 and 16-20 stand rejected under 35 U.S.C. §112, first paragraph, as containing subject matter not disclosed in the specification. Applicant respectfully traverses this rejection. Support for the central processing unit having an integrated memory controller is clearly provided in FIGURE 2. FIGURE 2 is a detailed view of central processing unit 20. Memory controller 30 and memory directory 18 are clearly shown to be within central processing unit 20. Applicant's specification at page 7, lines 5-7, particularly discloses that these components are integrated with memory 16 into a single device, processor 12. Thus, the specification provides clear support for the claim language. Therefore, Applicant respectfully submits that Claims 1-10 and 16-20 are in accordance with 35 U.S.C. §112, first paragraph.

Claims 1-10 and 16-20 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite. As pointed out above, FIGURE 2 and Applicant's specification provide ample support for the claimed invention. FIGURE 2 clearly shows a central processor 20 having a memory controller 30 and a memory directory 18 integrated, along with memory 16, into the single device of processor 12. Moreover, the term 'integrated' is clearly defined in the specification as being within a single device. Therefore, Applicant respectfully submits that Claims 1-10 and 16-20 are in accordance with 35 U.S.C. §112, second paragraph.

Claims 1, 2, and 4-20 stand rejected under 35 U.S.C. §102(b) as being anticipated by Kabemoto, et al. Independent Claims 1, 11, and 16 recites in general a processor including an integrated memory operable to provide/receive/store data, each processor including a central processing unit with an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory and at least one memory reference to data within an integrated memory of a different processor. By contrast, the Kabemoto, et al. patent shows processor and cache units separate from each other and a separate memory control module. Moreover, a directory memory is disclosed as being separate and apart from the processor. The Examiner seems to refer to processor element 14-1 of the Kabemoto, et al. patent in stating that each component of the claimed invention is found therein but has not shown how the processor 16-1 itself includes each component of the processor of the claimed invention. The processor element 14-1 of the Kabemoto, et al. patent includes a processor 16-1, a cache unit 18-1, and a snoop unit 20-1. The Examiner shows that the processor 16-1 of the Kabemoto, et al. patent includes a memory 36 and 38 but readily admits that a memory controller 35 and a memory directory 40 of the Kabemoto, et al. patent are not included in its processor 16-1 by showing that the memory controller 35 and the memory directory 40 are in the cache unit 18-1 which is separate and apart from the processor 16-1. As a result, the processor of the Kabemoto, et al. patent does not include the resources and functionality of the processor in the claimed invention. Thus, the Kabemoto, et al. patent does not have a processor that includes an integrated memory and a central processing unit with an

integrated memory controller and an integrated memory directory as provided by the claimed invention. Moreover, the Kabemoto, et al. patent does not disclose an ability to maintain at least one memory reference to data within an integrated memory of a different processor as required by the claimed invention. Support for the above recitation can be found at page 7, lines 14-20, of Applicant's specification. Therefore, Applicant respectfully submits that Claims 1, 2, and 4-20 are not anticipated by the Kabemoto, et al. patent.

Claims 1, 2, 5, 6, 9-11, and 13-17 stand rejected under 35 U.S.C. §102(e) as being anticipated by Chase, et al. Independent Claims 1, 11, and 16 recite in general a processor including an integrated memory operable to provide/receive/store data, each processor including a central processing unit with an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory and at least one memory reference to data within an integrated memory of a different processor. By contrast, the station 12 of the Chase, et al. patent equated by the Examiner as the claimed processor shows a processor 18 and a storage 21 with a cache 20 separate and apart from its processor 18. Thus, the storage 21 and cache 20 of the Chase, et al. patent are not integrated within its processor 18 as would be required by the claimed invention. Therefore, the Examiner has failed to show how the Chase, et al. patent has a processor with an integrated memory when the Chase, et al. patent specifically shows a separate processor 18 and a separate storage 20 that is not included within the processor 18.

The Chase, et al. patent expressly discloses a cache directory 16 in a directory server 17 that is separate and

apart from station 12 and its processor 18 and storage 21. The Chase, et al. patent clearly discloses the use of a cache directory 16 in a server 17 separate and remote from any of its stations 12 for use with cache 20 within station 12. The Chase, et al. patent clearly teaches away from any use of a directory within its station 12 and being integrated with its processor 18 let alone being integrated within a central processing unit as required by the claimed invention. Thus, the memory directory of the Chase, et al, patent is not integrated in a central processing unit of a processor as required by the claimed invention. In fact, the memory directory 16 is disclosed in the Chase, et al. patent as also being separate from a processor 18 within its directory server 17.

Further, the Chase, et al. patent provides no mention of a memory controller within station 12 or processor 18 let alone any integration of a memory controller within its processor 18. All of the portions of the Chase, et al. patent cited by the Examiner clearly show a memory controller being separate and apart from its corresponding processor. Thus, not only does the Chase, et al. patent fail to show a local memory integrated within a processor and a memory controller integrated within a central processing unit of a processor, there is also no support in the Chase, et al. patent for a memory directory also integrated in the central processing unit as required by the claimed invention.

Applicant's specification specifically shows that the term 'integrated' defines these elements as being within a single device, the processor. Thus, contrary to the Examiner's assertion, Applicant's specification clearly limits the claimed elements to a single device through the use of the word 'integrated' provided in the claims. The Chase, et al.

patent teaches away from this integration by having all of the claimed elements in separate devices. The processor of the Chase, et al. patent does not include the resources and functionality of the processor or the central processing unit in the claimed invention. As a result, the Examiner has not provided any teaching within the Chase, et al. patent to support the rejection of the claims. Thus, without a reference that discloses each and every limitation or a reference combinable with the Chase, et al. patent to support a rejection, the Chase, et al. patent by itself is insufficient to support a rejection of the claimed invention. Moreover, the Chase, et al. patent does not disclose an ability to maintain at least one memory reference to data within an integrated memory of a different processor as required by the claimed invention. Support for the above recitation can be found at page 7, lines 14-20, of Applicant's specification. Therefore, Applicant respectfully submits that Claims 1, 2, 5, 6, 9-11, and 13-17 are not anticipated by the Chase, et al. patent.

Claims 3, 10, 18, and 20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Chase, et al. Claim 1, from which Claims 3 and 10 depend, and Independent Claim 16, from which Claims 18 and 20 depend, have been shown above to be patentably distinct from the Chase, et al. patent. Therefore, Applicant respectfully submits that Claims 3, 10, 18, and 20 are patentably distinct from the Chase, et al. patent.

Claim 3 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Kabemoto, et al. Claim 1, from which Claim 3 depends, has been shown above to be patentably distinct from the Kabemoto, et al. patent. Therefore, Applicant

respectfully submits that Claim 3 is patentably distinct from the Kabemoto, et al. patent.

Applicant has shown above how the cited art fails to support a rejection of the claims. However, the Examiner continues to provide an improper omnibus rejection of the claims in contradiction to M.P.E.P. §707.07(d), making it difficult to understand the Examiner's position. The Examiner merely directs Applicant to specific portions of the cited art but fails to show how the specific portions of the cited art meet the terms of the claims. Applicant has read the specific portions of the cited art identified by the Examiner but respectfully submits that these cited portions fail to disclose each and every one of the elements of the claimed invention. Applicant respectfully requests the Examiner to provide a complete and proper analysis of the claims by showing how each and every limitation of each and every claim is possibly met by the prior art.

The changes to the specification made in the Request for Continued Examination stand objected to under 35 U.S.C. §132(a) as introducing new matter. Applicant respectfully submits that no new matter has been added into the specification. Changes to the specification have been made to provide consistency with what is clearly shown in FIGURE 2. FIGURE 2 clearly illustrates the make up of central processing unit 20 of processor 12. The element is labeled 20 as similarly provided in FIGURE 1. Memory directory 18 is consistently shown to be within element 20, the central processing unit, in both FIGUREs 1 and 2. Furthermore, the absence of memory 16 from FIGURE 2 is further consistent with FIGURE 2 being a depiction of central processing unit 20. Thus, changes to the specification have been appropriately made based on what is shown in FIGURE 2 without adding any new

matter. Therefore, Applicant respectfully submits that the changes made to the specification are in accordance with 35 U.S.C. §132(a).

The drawings stand objected under 37 C.F.R. §1.84(p)(5) for not including reference signs mentioned in the specification. FIGURE 2, in conjunction with FIGURE 1, includes the appropriate reference signs mentioned in Applicant's specification. Therefore, Applicant respectfully submits that the drawings are in accordance with 37 C.F.R. §1.84(p)(5).

The drawings stand objected under 37 C.F.R. §1.84(p)(5) for including reference signs not mentioned in the specification. Applicant's specification has been amended to be consistent with FIGURE 2. Therefore, Applicant respectfully submits that the drawings are in accordance with 37 C.F.R. §1.84(p)(5).

Claims 1-20 stand rejected under 35 U.S.C. §103(a) as being unpatentable over "The SGI Origin: A ccNUMA Highly Scalable Server" published by Laudon, et al. in view of "The MIPS R10000 Superscalar Microprocessor" published by Yeager. Independent Claims 1, 11, and 16 recite in general a processor including an integrated memory operable to provide/receive/store data, each processor including a central processing unit with an integrated memory controller operable to control access to the integrated memory and an integrated memory directory operable to maintain a plurality of memory references to data within the integrated memory and at least one memory reference to data within an integrated memory of a different processor. The Examiner indicates that the Laudon, et al. publication discloses the use of a R10000 processor and the Yeager publication discloses that the R10000 processor includes secondary caches and a CPU where the CPU has an

internal memory controller to control access to the secondary caches. Contrary to the Examiner's assertion, the Yeager publication fails to disclose that the R10000 CPU includes an integrated memory directory as required by the claimed invention. As shown in Figure 1, the Yeager publication clearly shows a directory separate from its CPU units. Moreover, there is no disclosure in the Yeager publication that the directory maintains memory references to data in its secondary caches.

The Examiner asserts that anyone of ordinary skill would know how to include the Mem & Dir onto the Hub Chip of the Laudon, et al. publication based on advances in fabrication in order to reduce time in propagating signals and provide savings in power. However, the Examiner fails to provide any support for such a conclusory statement. The Examiner has failed to provide any proof for such an assertion. In addition, there has been no showing that signal propagation delay and power are real problems contemplated in the prior art that would lead to the features of the claimed invention. Moreover, the Examiner has failed to show that such knowledge was available at the time of the present invention. In addition, the Examiner equates the Translation Look-aside Buffer of the Yeager publication as an integrated memory directory. However, the Translation Look-aside Buffer of the Yeager publication merely translates virtual addresses to physical addresses and fails to disclose any ability to maintain a memory reference to data stored in an integrated memory of a different processor as required by the claimed invention. Support for the above recitation can be found at page 7, lines 14-20, of Applicant's specification. Therefore, Applicant respectfully submits that Claims 1-10 are patentably

distinct from the proposed Laudon, et al. - Yeager combination.

Independent Claim 11 recites ". . . maintaining a list of memory references to the information in the local memory in a memory directory integrated with a central processing unit of the particular one of the plurality of processors; generating a request for data; determining whether the data is associated with information stored in the local memory and has a memory reference in the memory directory; forwarding the request to an external switch in response to the data not having a memory reference in the memory directory, wherein the data not having a memory reference to the local memory in the memory directory is stored in a remote memory . . ." By contrast, the Examiner merely rejects Claim 11 as failing to define over rejected Claims 1-10. However, Claim 11 does define over Claim 1 by being directed to an operation including steps not provided in Claim 1. Thus, the Examiner has failed to show that either of the Laudon, et al. or Yeager publications disclose the operation provided by Claim 11. Therefore, Applicant respectfully submits that Claims 11-15 are patentably distinct from the proposed Laudon, et al. - Yeager combination.

Independent Claim 16 recites ". . . a memory directory integrated in the central processing unit and operable to maintain memory references to data within the local memory, the memory directory operable to generate a data request for data not having a memory reference in the memory directory . . ." By contrast, as pointed out above with reference to Claim 1, the Yeager publication fails to disclose a memory directory integrated in its CPU and operable to maintain memory references to data in the local memory of the processor and to maintain at least one memory reference to data in an integrated memory of a different processor. Moreover, the

Yeager publication fails to disclose any directory operable to generate a data request for data not having a memory reference in the directory as required by the claimed invention. Therefore, Applicant respectfully submits that Claims 16-20 are patentably distinct from the proposed Laudon, et al. - Yeager combination.

CONCLUSION

Applicant has now made an earnest attempt to place this case in condition for allowance. For the foregoing reasons, and for other reasons clearly apparent, Applicant respectfully requests full allowance of all pending claims.

The Commissioner is hereby authorized to charge any fees or credit any overpayments associated with this Application to Deposit Account No. 02-0384 of BAKER BOTTS L.L.P.

Respectfully submitted,
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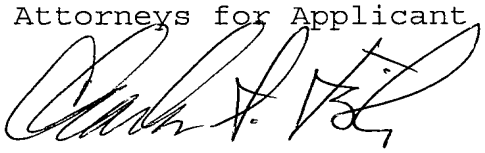

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